★★★　＜知的財産翻訳検定＞答案用紙　★★★

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※以下に解答を記入してください

問１.

TITLE OF THE INVENTION

VOLUME CONTROL CIRCUIT AND METHOD OF PORTABLE VEHICLE PHONE

BACKGROUND OF THE INVENTION

i)　Technical Field of The Invention

The present invention relates to a volume control circuit. Particularly, the present invention concerns with a volume control circuit for use in an apparatus, such as a portable vehicle phone, which can be installed at different locations.

ii)　Description of the Related Art

There are two cases in using a portable vehicle phone.　The phone can be set inside the vehicle, or the phone can be used carried along.　For the purpose of making and receiving calls with optimum volume regardless of the environment where the phone is used, the vehicle phone is generally provided with a volume

control circuit. More particularly, the volume is set large when the phone is set in a vehicle since environmental noise is large, while the volume is set small when the phone is carried along since environmental noise is small. However, a conventional volume control circuit requires volume adjustment every time there is a change in the use state of the phone. Therefore, the portable vehicle phone causes much trouble in making and receiving calls. Such a phone is not user-friendly.

One object of the present invention is to provide a volume control circuit with improved usability.

Another object of the present invention is to provide a volume control circuit that does not require volume adjustment each time there is a change in a use state of an apparatus.

WHAT IS CLAIMED IS:

1. A volume control circuit comprising:

an amplifying device that amplifies a voice signal;

first and second retaining devices that respectively retain a gain of the amplifying device in first and second predetermined setting values;

a state detecting device that detects a use state of an apparatus in which the volume control circuit is installed and outputs a state detection signal; and

a switching device that activates one of the first and

second retaining devices in response to the state detection signal.

2. The volume control circuit according to claim 1, further comprising

a setting device that selectively changes the first and second setting values of the first and second retaining devices in response to the state detection signal.

3. A volume control method comprising steps of:

retaining a plurality of gains respectively corresponding to a plurality of use states of an apparatus;

detecting one of the plurality of use states and outputting a state detection signal; and

selecting one of the gains corresponding to the state detection signal to amplify a voice signal in response to the state detection signal.

4. The volume control method according to claim 3, further comprising a step of

manually modifying the plurality of gains.

問2.

Operation of this pulse detection circuit is described hereafter. When the clock pulse to the input terminal CLK becomes Vdd level, the current is interrupted between FET T3 and T5, and the current flows between FET T4 and T6. Accordingly, Vss level is given to both ends of the capacity C3. When the clock pulse is changed to Vss level, the current flows to FET T3. Vdd level is given to one end of the capacity C3. At this time, if the point D is at Vss level, the circuit board of FET T5 becomes Vss level. Therefore, FET T5 is not operated and the current cannot flow. However, the potential of the other end of the capacity C3 increases as the one end of the capacity C3 increases to Vdd level. Accordingly, a PN junction constituted of the circuit board of FET T5 and the connection area on the side of the capacity C3 is biased in a forward direction. As a result, the current flows via the PN conjunction so as to charge the capacity C4. Due to a potential increase of the point D by the charging of the capacity C4, FET T5 is operated so that the current flows to FET T5. The current passing the capacity C3 flows through the source-drain path of FET T5. At this time, a connection electrode on the side of the capacity C3 of FET T5 serves as the source. The current is interrupted between FET T3 and T5 as the clock pulse becomes Vss level. Therefore, the point D is charged to a level lower than Vdd level.