２００６年度第３回知的財産翻訳検定＜英文和訳＞
【電気・電子工学分野】

※解答作成前に必ず下記の注意事項に目を通してください。

【解答にあたっての注意事項】
１．問題は３題あります。それぞれの問題の指示に従い、３題すべて解答してください。
２．問１の解答にあたっては図面を参照してください。
　　図面は本文上部にある「課題図表の表示・非表示」ボタンをクリックして閲覧できます。

問１．次のクレーム（Claims）を日本語に翻訳してください。なお、翻訳にあたってはクレームの後ろの明細書の記載（抜粋）および図面を参考にしてください。

Claims

1. A method for manufacturing a semiconductor device, comprising: forming a gate electrode on a semiconductor substrate with a gate insulation layer interposed therebetween; forming an insulation side wall at either lateral surface of the gate electrode; forming a source/drain region in a surface of the semiconductor substrate at either side of the gate electrode; forming a metal layer on the surface of the semiconductor substrate including the gate electrode; performing a plasma treatment on the metal layer; forming a capping material layer on the metal layer; performing an annealing process upon the semiconductor substrate to form a metal silicide layer on the surface of the semiconductor substrate at positions corresponding to the gate electrode and the source/drain region; and removing the capping material layer and the metal layer left unreacted with the gate electrode and the semiconductor substrate.

2. The method as set forth in claim 1, wherein the capping material layer is formed by depositing one of a titanium layer and a nitride titanium layer using one of physical vapor deposition and chemical vapor deposition.

3. The method as set forth in claim 1, wherein the forming of the metal layer, the plasma treatment, the forming of the capping material layer, and the annealing process are performed in the same chamber.

【参考】　明細書の記載（抜粋）

A device isolation layer 32 is formed on a semiconductor substrate 31 by a LOCOS process. The semiconductor substrate 31 is thermally oxidized to form a gate oxide layer 33.

A poly-silicon layer is deposited on the gate oxide layer 33, and is selectively etched to form a gate electrode 34. Low-density impurity ions are implanted into a surface of the semiconductor substrate 31 at opposite sides of the gate electrode 34 to form a LDD region 35.

An insulation layer is deposited on the surface of the semiconductor substrate 31 and is subjected to an etch-back process to form an insulation sidewall 36 at either lateral surface of the gate electrode 34. High-density impurity ions are implanted into the surface of the semiconductor substrate 31 to form a source/drain impurity region 37.

The semiconductor substrate 31 is transferred into a chamber of a specific apparatus, for example, a physical vapor deposition or a chemical vapor deposition apparatus to form a metal layer 38.

A capping material layer 39 formed of any one of a titanium layer and a nitride titanium layer is formed on the metal layer 38 using physical vapor deposition or chemical vapor deposition in the same chamber. (FIG. 2F)

The semiconductor substrate 31 is subjected to an annealing process under nitrogen or ammonia atmosphere in the same chamber to form a metal silicide layer 40 on the surface of the semiconductor substrate 31 at positions corresponding to the gate electrode 34 and the source/drain impurity region 37. (FIG. 2G)

The metal layer 38 that remained unreacted with the semiconductor substrate 31 and the gate electrode 34, and the capping material layer 39 formed thereon, are removed via a wet etching process. (FIG. 2H)

課題図表【電気】

FIG. 2F

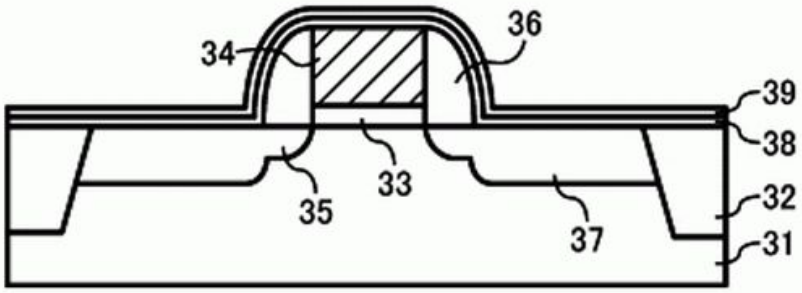


FIG. 2G

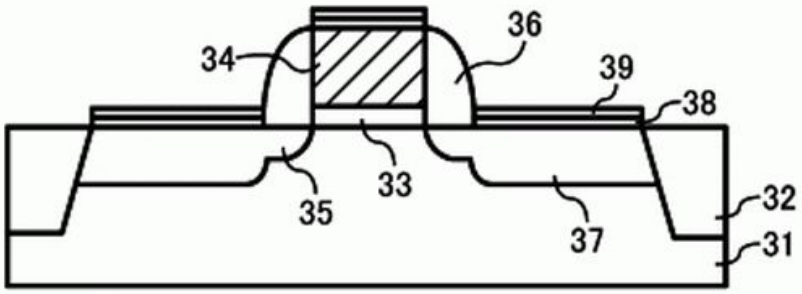
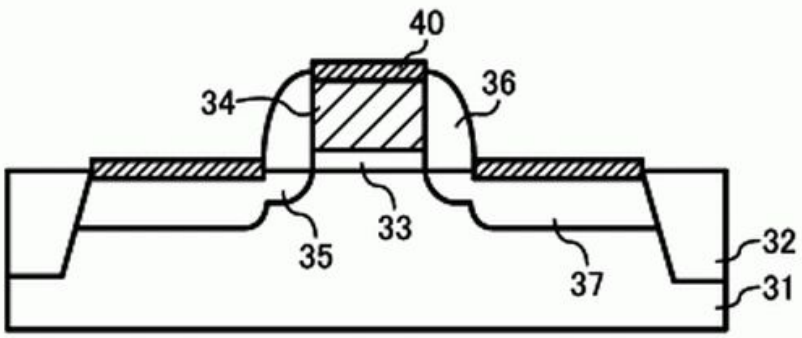


FIG. 2H



問２．次の文を日本語に翻訳してください。なお、翻訳文にもパラグラフ番号を付けてください。

DESCRIPTION OF THE RELATED ART

[0001] Modern electronic devices often use microprocessors or other digital circuits which require one or more clock signals for synchronization. For example, a clock signal permits the precise timing of events in the microprocessor. Typical microprocessors may be regulated or synchronized by a free-running oscillator, such as one driven by a crystal, an LC-tuned circuit, or an external clock source.

[0002] Over the years, clocking rates have continued to increase, and currently clock rates in personal computes may exceed 2.0 gigahertz (GHz). As clock rates increase, the circuits generating and processing the clock signals are susceptible to generating and radiating electromagnetic interference (EMI) emission. The spectral components of the EMI emissions typically have peak amplitudes at harmonics of the fundamental frequency of the clock circuit.

[0003] In order to comply with government limits on EMI emissions, spread spectrum clock generation (SSCG), such as that disclosed in U.S. Pat. No. 5,631,920, has been used to reduce EMI emissions. In summary, an SSCG circuit may include a clock pulse generator for generating a series of clock pulses, and a spread spectrum modulator for frequency modulating the clock pulse generator to broaden and flatten EMI spectral components which would otherwise be produced by the clock pulse generator.

問３．次の文を日本語に翻訳してください。なお、翻訳文にもパラグラフ番号をつけてください。

DETAILED DESCRIPTION

[0101] With reference to FIG. 1, a print system 2 is explained. In the current embodiment, a system controller 4 including a user interface having a screen (not shown) is connected to an Ethernet hub 6 via the serial communications channel (or command control bus) 8. The Ethernet hub 6 is also linked to any number of MFFA (multiple feeding and finishing architecture) modules 10 and interface converters 14 via the communications channel 8.

[0102] The communications channel 8 is typically Ethernet-based, 10 base T in the iGen family, and is used for communication between the modules 10 and to the system controller 4. "10 Base T" refers to a type of cable used to connect nodes on an Ethernet network. The number "10" refers to the transfer rate used on standard Ethernet, 10 Mbps.

[0103] The term "Base" means that the network uses baseband communication rather than broadband communication. The letter "T" stands for twisted pair. The 10 Base T standard uses a twisted-pair cable with a maximum length of 100 meters. The communications channel 8 allows full bidirectional communication between the system controller 4 and the MFFA modules 10.