２００７年度第５回知的財産翻訳検定＜英文和訳＞
【電気・電子工学分野】

※解答作成前に必ず下記の注意事項に目を通してください。

【解答にあたっての注意事項】
１．問題は３題あります。それぞれの問題の指示に従い、３題すべて解答してください。
２．問１および問３の解答にあたっては図面を参照してください。
　これらの図は本文上部にある「課題図表の表示・非表示」ボタンをクリックして
　閲覧できます。

問１．次のクレーム１と２をそれぞれ日本特許明細書の請求項１と請求項２として、＜スタート＞から＜エンド＞までを翻訳しなさい。参考資料として FIG．１とその説明を添付していますが、これらは翻訳対象ではありません。

＜スタート＞
1.　An active matrix display device, comprising:
　　sets of row and column address conductors;
　　a row and column array of electro-optic display elements operable to produce a display, each of which is connected in series with a two terminal non-linear switching device between a row conductor and a column conductor; and
　　a drive circuit connected to the sets of row and column address conductors for applying selection signals to the row address conductors to select the rows of display elements and data signals to the column address conductors to drive the selected display elements to produce a required display effect,
　　wherein the data signals comprise pulse width modulated signals whose width determines a desired grey scale output from a display element, and
　　wherein the drive circuit is adapted to provide selection signals which comprise voltage pulse signals whose magnitude increases to a maximum voltage amplitude such that the current flowing through a non-linear switching device during the application of a selection signal tends towards a substantially constant value.

2. An active matrix display device according to claim 1, characterized in that the duration of a selection signal applied to a row address conductor is predetermined and defines an address period for a display element and in that a data signal applied to a column address conductor determines the end of an interval within the display element address period in which current flows through the non-linear switching device to drive the display element.
＜エンド＞

＊参考資料
Referring to FIG. 1, the display device, which is intended for datagraphic display purposes, comprises an active matrix addressed liquid crystal display panel 10 of conventional construction and consisting of m rows (1 to m) with n display elements 12 (1 to n) in each row. Each display element 12, here represented as a capacitor, comprises a liquid crystal display element consisting of two spaced electrodes with twisted nematic liquid crystal material disposed therebetween, and is connected electrically in series with a bidirectional non-linear resistance switching device 15 between a row address conductor 16 and a column address conductor 17. The non-linear device 15 exhibits a substantially symmetrical threshold characteristic and functions in operation as a switching element. The display elements 12 are addressed via the sets of row and column conductors 16 and 17 which are carried on respective opposing faces of two, spaced, glass supporting plates (not shown) also carrying the opposing electrodes of the liquid crystal display elements. The devices 15 are provided on the same plate as the set of row conductors 16 but could instead be provided on the other plate and connected between the column conductors and the display elements.

【問１・課題図表（電気・電子工学)】

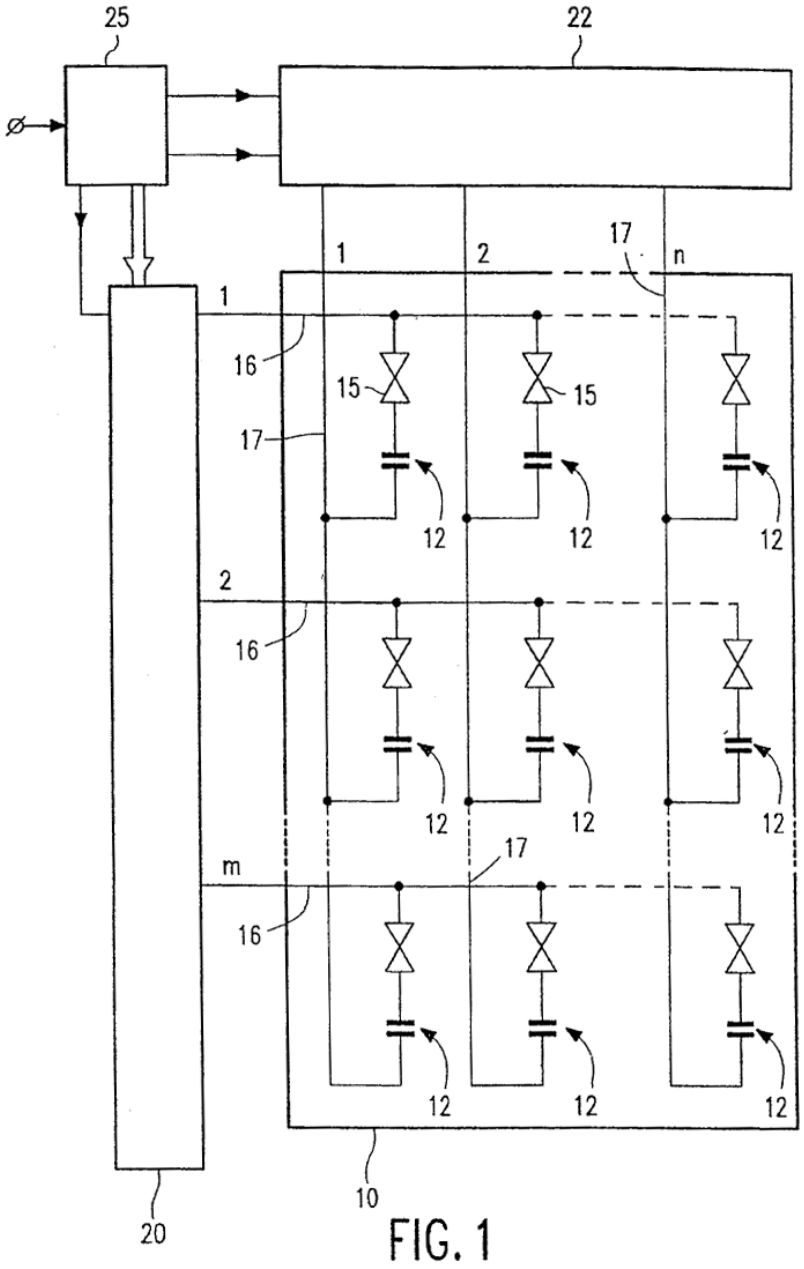

FIG. 1

問２．次の米国特許明細書中の背景技術にかかわる記載内容について翻訳しなさい。

＜スタート＞

As might be expected, the very small components on MEMS devices are sometimes very fragile and subject to being easily damaged or degraded even in normal operation. For this reason, a protective cover is often employed even when the device is ultimately to be disposed in a relatively isolated location. This cover is designed to protect the

components of the MEMS device from moisture and from deleterious materials, as well as from impact by other objects during assembly or operation. In the case of an optical MEMS device, the cover will normally be transparent, or at least clear enough to allow passage of the requisite amount of light. The cover is almost always a separate component, and must be securely mounted in such a manner so as to facilitate the function of the cover and of the device itself. As background for the present invention, an exemplary MEMS device will now be described in greater detail.
＜エンド＞

問３．次の米国特許明細書中の実施例の説明にかかわる記載内容について翻訳しなさい。参考資料として FIG．2 を添付します。

＜スタート＞
This embodiment also comprises a bidirectional shift register which contains a plurality of one bit shift registers. The number of one bit shift registers is equal to the number of bottom stack registers, S2 through S9 located below the S register. Each one bit shift register is connected to its corresponding S2 through S9 stack register as shown in FIG. 2. The one bit shift registers are electrically interconnected in an alternating pattern, such that the S2 through S9 registers of the stack function in the sequential circular interconnect pattern given by S2→S4→S6→S8→S9→S7→S5→S3→S2 as shown in FIG. 2. This sequential selection of bottom stack registers operates in a circular repeating pattern. The interconnecting wires of the one bit shift registers never span more than three adjacent shift registers, which avoids the need for a long wire connecting the bottom shift register to the top shift register. These shorter wires require a smaller driver, and buffering is also minimized. The embodiment given uses eight additional stack registers for the circular register array. However, other combinations of bottom registers used in multiples of four can also be utilized.
＜エンド＞

【問 3・課題図表（電気・電子工学）】

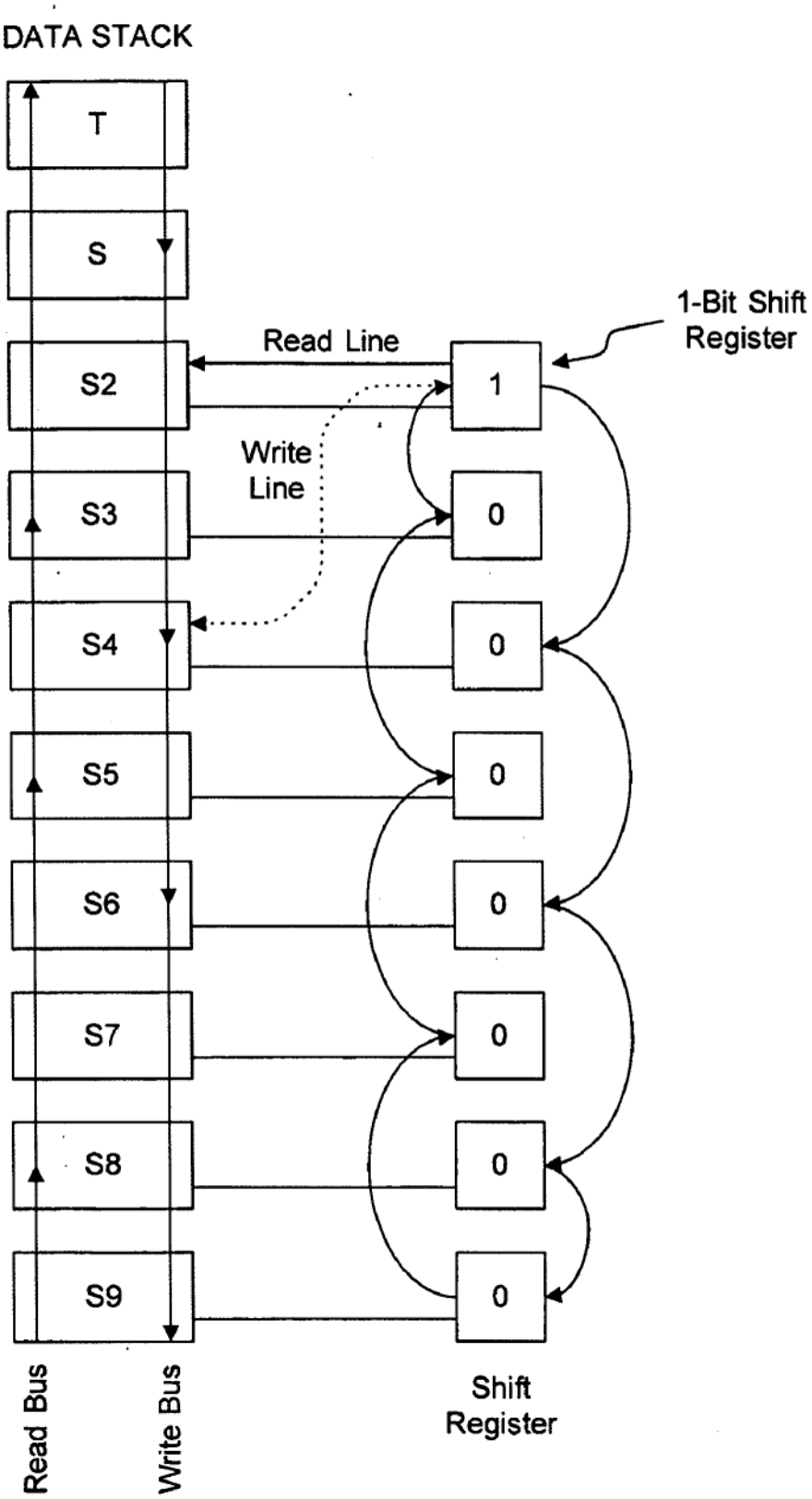

Fig. 2