★★★ ２００８年度第７回知的財産翻訳検定＜英文和訳＞ ★★★

≪１級 -電気・電子工学-≫

【解答にあたっての注意】

１．＜スタート＞ から＜エンド＞ までを英訳してください。

２．問題は３題あります。それぞれの問題の指示に従い、３題すべて解答してください。

３．解答語数に特に制限はありません。

４．課題文に段落番号がある場合、これを訳文に記載してください。

５．課題に図面が添付されている場合、該当する図面を参照してください。

★「課題図表の表示／非表示」リンクで表示

【問１】次の英文はある米国特許明細書中の独立クレームです。本クレームを日本特許明細書の請求項１として翻訳しなさい。

参考資料として FIG. 1 とその説明を添付していますが、これらは翻訳対象ではありません。

＜スタート＞

1. A circuit, comprising:

a multiple clock reference generator serving as a source of N reference clock frequencies, where N is an integer greater than one;

N frequency extender circuits receiving the N reference clock frequencies and generating N frequency extended output clock signals therefrom;

a plurality of N seed slewers producing N seed update values;

a plurality of N seed registers each one receiving one of the N seed update values and producing N seed masks therefrom;

a plurality of N logic circuits each receiving one of the N seed masks and one of the N frequency extended output clock signals, each of the N logic circuits producing a pseudorandom sequence from the seed mask and the frequency extended output clock signal;

a plurality of N correlators, each said correlator receiving one of the N pseudorandom sequences and correlating the pseudorandom sequence with a CDMA pilot I channel signal to produce a plurality of N offsets; and

a reconfigurable processor controlling the N frequencies produced by the multiple reference clock generator.

＜エンド＞

＊参考資料

In accordance with certain embodiments consistent with the present invention, certain of the above components can be assembled to provide a multiple user reconfigurable CDMA processor which either permits multiple sequence generation on the same channel or multiple sequences for multiple channels.

Such an arrangement is depicted by way of exemplary embodiment in FIG. 1. In this embodiment, a multiple frequency generator 230 can be used to generate multiple clock frequencies from a single reference input as previously described. Such multiple references from a single reference input can be determined by control processor 950, which may be embodied within a reconfigurable processor array such as 240, or may be any other suitable control processor without limitation. The multiple clock frequencies F1, F2 through FN can serve as multiple reference clock frequencies that can be extended by use of frequency extender circuits 954 such as those depicted as 500 or 501 in order to produce frequency extended output clock output clock signals.

A bank of seed slewers 958, which may be embodied within the same logic as multiple reference clock generator 240, produce a plurality of N seed updates that are updated at suitable clock rate to produce a corresponding plurality of N seed mask values from a bank of N seed registers 962. Each of the N seed masks from seed registers 962 are combined by one of N logic circuits 966 with an appropriate one of the N outputs of the frequency extender circuits of 954 (operating, for example in the same manner as gates 612, 616, through 620 and 630 of recursive sequence generator 600 of FIG. 9) to produce a N separate PN codes, one at each output of each of the N logic circuits of the bank of logic circuits 966. Each of these N-PN codes 990-1, 990-2 through 990-N can then be applied to a separate correlator within a bank of correlators 970. The PN codes are thus correlated with the Pilot I-channel information at the N correlators to produce M offset values. These M offset values can then be used in a multiple user reconfigurable CDMA processor which either permits multiple sequence generation and correlation on the same channel or multiple sequences and correlation for multiple channels.

【問２】次の米国特許明細書中の背景技術にかかわる記載内容について翻訳しなさい。

＜スタート＞

Traditionally, performing a floating point mathematical operation and normalizing the result is a slow and tedious process. After computational circuitry performs a floating point operation on two operands, the result must be normalized so as to contain a "one" in the most significant bit (MSB) of the mantissa. A leading zero counter (LZC) or one detector is often used to count the number of leading zeroes in the mantissa. The floating point result is normalized by shifting the mantissa the number of bits indicated by the LZC. The result must also be converted to a signed magnitude form and rounded to ensure sufficient accuracy and precision. Typically, the steps of converting and rounding require two separate passes through an adder circuit.

Both computation and normalization steps are time consuming. The computation step is delayed due to the carry propagation of data during the floating point operation. In prior art systems, the normalization process cannot begin until after the floating point operation is complete Current arithmetic systems are thus inherently slow since the computation and normalization steps must be performed sequentially.

＜エンド＞

【問３】次の米国特許明細書中の実施例の説明にかかわる記載内容について翻訳しなさい。参考資料として FIG. 10 を添付します。

＜スタート＞

The present disclosure describes a method and apparatus for collecting antenna position measurements using phase measurements from a plurality of GPS sensors mechanically connected to structurally stiff locations on a large radar antenna, and combining the plurality of target motion measurements to improve overall antenna orientation accuracy as compared to previous approaches.

FIG. 10 shows an antenna 101 of the prior art where the azimuth

orientation of the antenna is measured by a rotating angle transducer 103 capable of reporting the antenna azimuth angle position. From geometric considerations, if the uncertainty, or error of the reported azimuth angle from transducer 103 is θ,
then the azimuth error at range R is:

Azimuth Error=R sinθ.

For example, for R=50 nautical miles (nm), and θ=10 milliradians, (about 1/2 degree) the resulting
azimuth error is approximately:

50 nm*6076.1 ft/nm*0.01 radians=3038 ft

Thus, mechanical angle transducers having an accuracy in the order of 1/2 degree are too coarse, or inaccurate to provide a meaningful indication of antenna azimuth position in radar systems requiring
azimuth (cross range) accuracy in the order of 2 ft. Even a ten fold improvement in measuring θ by an angle transducer 103 would not be satisfactory in such a scenario: Given these high errors and associated
limitations in deriving accurate images, it is desired to implement a viable method of measuring antenna orientation around an axis, applicable to both azimuth and elevation in the case of relatively large antennas having an energy receiving area in the order of 20 meters by 20 meters.
＜エンド＞

【電気・電子工学　問１】

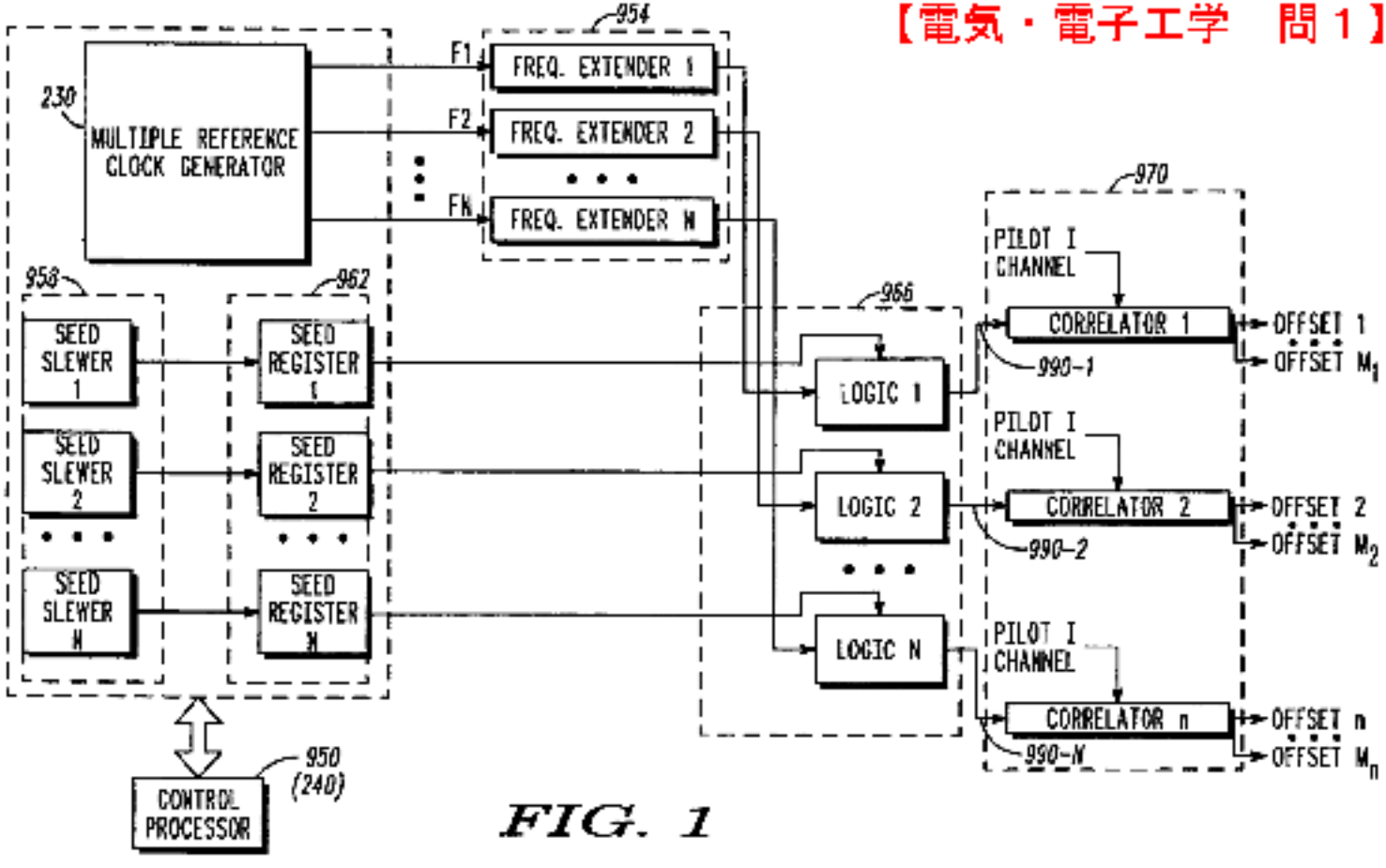

FIG. 1

【電気・電子工学　問3】

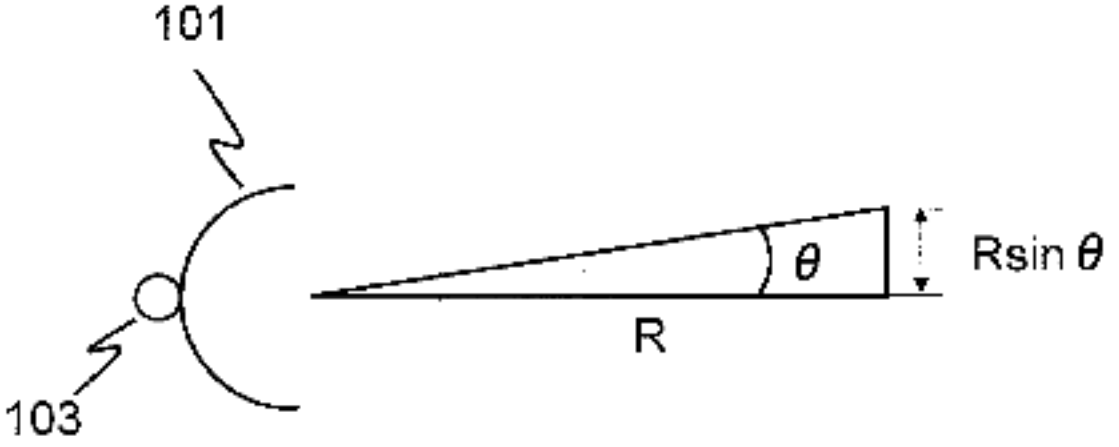

FIG. 10
PRIOR ART